A

UNITED STATES CONTINUING UTILITY PATENT APPLICATION

under 37 C.F.R. § 1.53(b)

Atty. Docket No. 1701.00021
Customer No. 22907

Director of Patents
Box Patent Applications
Washington, D.C. 20231

Enclosed herewith is a continuing patent application and the following papers:

First Named Inventor (or application identifier): Yusuke Kohyama

Title of Invention: STACKED CAPACITOR-TYPE SEMICONDUCTOR STORAGE DEVICE AND MANUFACTURING METHOD THEREOF

☐ Continuation
■ Divisional
☐ Continuation-in-Part

of prior application No. 08/720,032, filed September 27, 1996

1. ■ Specification 37 pages (including specification, claims, abstract)

2. ■ Declaration/Power of Attorney:
   - ■ Copy from Prior Application (for continuation or divisional application)
   - ☐ Newly Executed Declaration (for CIP application)
   - ☐ Deferred under 37 C.F.R. § 1.53(f)
   - ☐ Deletion of Inventor(s) - Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b)
   - ■ Incorporation by Reference - The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein

3. ■ 13 Distinct sheets of ■ Formal ☐ Informal Drawings

4. ■ Preliminary Amendment

5. ■ Information Disclosure Statement
   - ■ Form 1449
   - ☐ A copy of each cited prior art reference

6. ■ Assignment
   - ☐ Assignment with Cover Sheet attached
   - ■ Assignment filed in prior application. Application assigned to: **Kabushiki Kaisha Toshiba**

7. ■ Priority is hereby claimed under 35 U.S.C. § 119 based upon the following application(s):

Country	Application Number	Date of Filing (day, month, year)
Japan	7-254218	29 September 1995

8. ☐ Priority document(s)

9. ☐ Small Entity Statement
   - ☐ Small Entity Statement was filed in prior application, Small Entity Status is still proper and desired
   - ☐ is attached
   - ☐ is no longer claimed

10. ☐ Microfiche Computer Program (Appendix)

11. ☐ Nucleotide and/or Amino Acid Sequence Submission
    - ☐ Computer Readable Copy
    - ☐ Paper Copy (identical to computer copy)
    - ☐ Statement verifying identity of above copies

12. Calculation of Fees after entry of Preliminary Amendment:

FEES FOR	EXCESS CLAIMS	FEE	AMOUNT DUE
Basic Filing Fee (37 C.F.R. § 1.16(a))			$690.00
Total Claims in Excess of 20 (37 C.F.R. § 1.16(c))	0	18.00	$0.00
Independent Claims in Excess of 3 (37 C.F.R. § 1.16(b))	0	78.00	$0.00
Multiple Dependent Claims (37 C.F.R. § 1.16(d))	0	260.00	$0.00
Subtotal - Filing Fee Due			$690.00
	MULTIPLY BY		
Reduction by 50%, if Small Entity (37 C.F.R. §§ 1.9, 1.27, 1.28)	0		$0.00
TOTAL FILING FEE DUE			$690.00
Assignment Recordation Fee (if applicable) (37 C.F.R. § 1.21(h))	0	40.00	$0.00
GRAND TOTAL DUE			**$690.00**

13. PAYMENT is:

■ included in the amount of the GRAND TOTAL by our enclosed check. A general authorization under 37 C.F.R. § 1.25(b), second sentence, is hereby given to credit or debit our Deposit Account No. 19-0733 for the instant filing and for any other fees during the pendency of this application under 37 C.F.R. §§ 1.16, 1.17 and 1.18

☐ not included, but deferred under 37 C.F.R. § 1.53(f).

14. All correspondence for the attached application should be directed to:

Customer No. 22907
Banner & Witcoff, Ltd.
1001 G Street, N.W.
Washington, D. C. 20001-4597
Telephone: (202) 508-9100
Facsimile: (202) 508-9299

15. Other: ______

Date: August 3, 2000

By: Guy D. Yelenkh #35,509
for Joseph M. Potenza
Reg. No. 28,175

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Yusuke Kohyama et al. Atty. Docket: 1701.00021

Serial No.: Rule 1.53(b) Divisional of 08/720,032 Art Unit: 2835

Filed: Herewith Examiner: H. Duong

For: **STACKED CAPACITOR-TYPE SEMICONDUCTOR STORAGE DEVICE AND MANUFACTURING METHOD THEREOF**

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination on the merits and in conjunction with the divisional application filed herewith pursuant to 37 C.F.R. § 1.53(b), please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please amend the specification as follows:

Page 1, before line 1, insert --This application is a divisional of prior application serial no. 08/720,032 filed September 27, 1996.--.

Page 1, line 12, before "DRAM" insert --a--;

line 26, delete "there suggests" and after "cell" insert --is suggested as--.

Page 2, line 12, change "an" to --a--.

Page 3, line 14, change "an" to --a--.

Page 4, line 10, change "yielding" to --yield--;

line 20, change "excellent yielding" to --an excellent yield--;

line 25, change "comprising" to --comprises--.

Page 5,	line 14, change "comprising" to --comprises--.
Page 6,	lines 12, 16, 20, and 26, after "show" insert --a--.
Page 7,	lines 2, 6, 9 and 14, after "manufacturing" insert --according to--;
	lines 18 and 21, after "manufacturing" insert --according to a--;
	line 23, after "shows" insert --a--.
Page 8,	line 8, delete "on" and insert --with--.
Page 9,	line 19, after "CH," insert --a--;
	line 21, after "show" insert --a--.
Page 10,	line 5, delete "is used".
Page 11,	line 6, after "nitride film" insert --,--;
	line 10, after "show" insert --a--.
Page 12,	line 10, change "space" to --spacer--.
Page 13,	line 8, before "fourth" insert --a--;
	line 9, change "on" to --with--;
	line 17, after "manufacturing" insert --according to--.
Page 14,	line 6, change "patter" to --pattern--;
	line 14, change "7C" to --7A--;
	line 22, change "cilicide" to --silicide--;
	line 27, change "an" to --a--.
Page 15,	line 1, change "as" to --of--.
Page 18,	line 4, change "know" to --known--;

line 25, change "yielding" to --yield--.

Page 19, line 3, delete "a higher" and insert --the--;

line 5, after "show" insert --a--.

Page 20, line 12, change "decrease" to --a decrease in--;

line 19, after "show" insert --a--.

Page 21, line 18, after "shows" insert --a--;

line 24, delete "as";

line 25, delete "well as" and insert --and--; change "is" to --are--.

IN THE CLAIMS:

Please cancel claims 1-19.

REMARKS

Claims 20-29, which were not elected in the parent application, are presented for examination.

The specification has been amended to correct various informalities.

Favorable consideration and allowance of the instant application are respectfully requested.

Respectfully submitted,

Gary D. Fedorochko #35,509

Date: August 3, 2000

for Joseph M. Potenza
Reg. No. 28,175

BANNER & WITCOFF, LTD.
Eleventh Floor
1001 G Street, N.W.
Washington, D.C. 20001-4597
(202) 508-9100

APPLICATION FOR

UNITED STATES LETTERS PATENT

SPECIFICATION

Inventors: Yusuke Kohyama

Takashi Ohsawa

Shizuo Sawada

Title of the Invention:

STACKED CAPACITOR-TYPE SEMICONDUCTOR STORAGE DEVICE AND MANUFACTURING METHOD THEREOF

Background of the Invention

1. Field of the Invention

The present invention relates to a cell structure of dynamic RAM (i.e. DRAM), for example, more specifically, a STC (Stacked Capacitor)-type semiconductor storage device in which a memory cell capacitor is formed above a bit line so as to be self-aligned with the bit line, and relates to a manufacturing method thereof.

2. Description of the Related Art

Recently, a semiconductor storage device, particularly, DRAM has been integrated greatly. Accordingly, a percentage of a unit storage element is showing a tendency to further increase. For this reason, a three-dimensional memory cell capacitor and a three-dimensional memory cell transistor are indispensable for obtaining enough capacity (not less than 20 fF) to read/write. As a result, a cell structure using a trench-type capacitor or STC-type capacitor is generally used.

In addition, in the cell using the STC-type capacitor, a technique for forming a memory cell capacitor so that it is self-aligned with a bit line is important to greater-scale integration. As a method of manufacturing the conventional STC-type capacitor, there suggests a memory cell described in, for example, M. Fukumoto et al., "Stacked capacitor cell technology

for 16M DRAM using double self aligned contacts", ESSDERC 90, pp. 461-464, 1990. FIGS. 13 through 15 show its example.

FIG. 13 shows a plan view of the memory cell. In FIG. 13, 201 is a channel region, 202 is a gate electrode pattern, 203 is a bit line contact, 204 is a bit line pattern, 205 is a storage node contact pattern, and 206 is a storage node electrode pattern.

FIGS. 14A through 14C show manufacturing steps of a cross-sectional view taken along line 14-14 in FIG. 13. As shown in FIG. 14A, an element separating oxide film 52, an MOS transistor for transmitting data, not shown, a first inter-layer insulating film 53, a bit line contact, not shown, a bit line 54, and a second inter-layer insulating film 55 made of BPSG film are formed on a semiconductor substrate 51. Next, a storage node contact 56 which reaches the semiconductor substrate 51 is formed in the first and second inter-layer insulating films 53 and 55 which is located between the bit lines 54-54 by the known lithography method and the RIE (Reactive Ion Etching) method.

Next, As shown in FIG. 14B, an HTO (High Temperature Oxide) film 57 is deposited over the whole surface, and the whole surface is etch-backed by the RIE method. Then, as shown in FIG. 14C, a side wall spacer 58 constituted by the HTO film 57 is formed on the first and second inter-layer insulating films

exposed in the storage node contact 56.

If the storage node contact pattern 205 shown in FIG. 13 is not aligned with the bit line pattern 204, the following problems arise. As shown in FIG. 15A, when the storage node contact 56 is formed, the bit line 54 is exposed from the first and second inter-layer insulating films 53 and 55. In this state, as shown in FIG. 15B, the HTO film 57 is deposited on the whole surface, the whole surface is etch-backed by the RIE method. Then, as shown in FIG. 15C, the side wall spacer 58 is formed in the storage node contact 56 so as to be on the bit line 54 and the side wall of the second inter-layer insulating film 55. However, since a part of the bit line 54 is exposed from an gap of the side wall spacer 58, the storage node, not shown, which is formed later and the bit line 54 are short-circuited.

In addition, when the whole surface of the HTO film 57 is etch-backed, since the HTO film 57 and the second inter-layer insulating film 55 are made of silicon oxide, sufficient selectivity cannot be obtained. Therefore, it becomes difficult to control thicknesses of the insulating film on the bit line 54 and the second inter-layer insulating film 55.

Furthermore, when the storage node contact 56 is formed, since a contact opening and a contact gap are minute, it is difficult to form a resist pattern.

Moreover, the storage node contact 56 does not have a desired shape, i.e. square shape, and as shown by broken lines in FIG. 13, it has a circular shape. The circular shape has a diameter which is a minimum dimension of the diameter when the storage node contact 56 is inscribed in a square pattern. The contact area decreases, thereby increasing contact resistance. Moreover, since the storage node contact 56 reaches the semiconductor substrate 51, an aspect ratio becomes large. As a result, yielding of the contact opening is not efficient, and thus it is difficult to plug up the storage node.

Summary of the Invention

It is an object of the present invention to provide a semiconductor storage device which is capable of preventing a short-circuit of a contact and a wiring, forming the contact so that the contact is self-aligned, and securely controlling a thickness of a film formed on the wiring, forming a fine contact with excellent yielding of an opening of the contact, and filling up the contact, and relates to a manufacturing method thereof.

In order to achieve the above object, a semiconductor storage device of the present invention comprising:

a first insulating film formed on a semiconductor substrate;

first and second wirings arranged on the first insulating film at a predetermined interval, the first and second wirings composed of a conductive film, and a second insulating film on the conductive film;

a contact hole formed between the first and second wirings, and on the first insulating film between the first and second wirings; and

a third insulating film formed in the contact hole, the third insulating film being formed at least on a side wall of the conductive film and a side wall of the first insulating film.

In addition a method of manufacturing a semiconductor storage device comprising the steps of:

forming a first insulating film on a semiconductor substrate;

forming a conductive film on the first insulating film;

forming a protective film on the conductive film;

etching the protective film and conductive film locally and forming first and second wirings;

forming a second insulating film between the first and second wirings;

etching the second insulating film and first insulating film locally by using the protective film as a mask and forming a contact hole between the first and second wirings; and

forming a third insulating film at least on a side

wall of the conductive film and on a side wall of the first insulating film in the contact hole.

Brief Description of the Drawings

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently preferred embodiments of the invention and, together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the invention.

FIGS. 1A through 1D are cross-sectional views which show first embodiment of the present invention, more specifically, the step of manufacturing of a semiconductor device;

FIGS. 2A through 2C are cross-sectional views which show second embodiment of the present invention, more specifically, the step of manufacturing of a semiconductor device;

FIG. 3 is a plan view which shows a mask pattern which is applied to third embodiment of the present invention;

FIGS. 4A through 4C show the third embodiment of the present invention, more specifically, they are cross sectional views taken along a line 4-4 in FIG. 3;

FIG. 5 is a plan view which shows a mask pattern which is applied to fourth embodiment of the present invention;

FIGS. 6A through 6J show the steps of manufacturing the fourth embodiment of the present invention, more specifically they are cross-sectional views taken along a line 6-6 in FIG. 5;

FIGS. 7A through 7G show the steps of manufacturing the fourth embodiment of the present invention, more specifically they are cross-sectional views taken along a line 7-7 in FIG. 5;

FIGS. 8A and 8B show the steps of manufacturing the fourth embodiment of the present invention, more specifically they are cross-sectional views taken along a line 8-8 in FIG. 5;

FIGS. 9A through 9E show the steps of manufacturing the fourth embodiment of the present invention, more specifically they are cross-sectional views taken along a line 9-9 in FIG. 5;

FIGS. 10A and 10B are cross-sectional views which show the steps of manufacturing fifth embodiment of the present invention;

FIGS. 11A through 11C are cross-sectional views which show the steps of manufacturing sixth embodiment of the present invention;

FIG. 12 is a cross-sectional view which shows seventh embodiment of the present invention;

FIG. 13 is a plan view which shows a conventional memory cell;

FIGS. 14A through 14C show the steps of

manufacturing the conventional memory cell, more specifically, they are cross-sectional views taken a line 14-14 in FIG. 13; and

FIGS. 15A through 15C are cross-sectional views witch show problems of the conventional memory cell.

Detailed Description of the Preferred Embodiments

The following describes embodiments of the present invention on reference to the drawings.

FIGS. 1A through 1D show the first embodiment of the present invention. As shown in FIG. 1A, a first insulating film 1 made of silicon oxide is formed on a semiconductor substrate 11. A conductive film 2, such as tungsten (W), a second insulating film 3 made of silicon oxide, and a third insulating film 4 made of silicon nitride are formed on the first insulating film 1. Thereafter, the third insulating film 4, the second insulating film 3 and the conductive film 2 are patterned by using a desired wiring pattern so that a wiring L is formed.

Next, as shown in FIG. 1B, a fourth insulating film 5 made of silicon oxide is deposited on the whole surface, and the surface is planarized by the CMP (Chemical Mechanical Polishing) method. As shown in FIG. 1C, a photo-resist 6 is formed on the fourth insulating film 5 by using a desired contact hole pattern. The fourth and first insulating films 5 and 1 are etched by the RIE method under an etching condition

that a selectivity to the fourth and first insulating films 5 and 1 and the third insulating film 4 is high, and then a contact hole CH is formed.

Next, the resist 6 is removed, and the fifth insulating film 7 is deposited on the whole surface. The fifth insulating film 7 is etch-backed by the RIE method, and as shown in FIG. 1D, a side wall spacer 7a composed of the fifth insulating film 7 is formed on a side wall of the contact hole CH. The side wall spacer 7a is formed on side walls of the first insulating film 1, the conductive film 2, the second insulating film 3, the third insulating film 4 and the fourth insulating film 5.

Since the conductive film 2 is protected by the third insulating film 4, at the timing of etching it by the RIE method, even if alignment is not obtained on a mask, the conductive film 2 is not exposed. Therefore, even when a conductive layer is formed in the contact hole CH, short-circuit between the conductive film 2 and the conductive layer can be prevented.

FIGS. 2A through 2C show second embodiment of the present invention. Here, the parts described in the first embodiment are indicated by the same reference numerals. The manufacturing steps up to the formation of a desired wiring L are the same as the first embodiment. After the wiring L is formed, the fourth insulating film 5 is deposited on the whole surface,

and as shown in FIG. 2A, the surface of the fourth insulating film 5 is planarized by the CMP method. At this time, the fourth insulating film 5 is planarized with the upper surface of the third insulating film 4 by using the third insulating film 4 is used as a stopper of CMP.

Next, the photo-resist 6 is formed by using a desired contact hole pattern. As shown in FIG. 2B, the fourth and first insulating films 5 and 1 are etched by the RIE method under the etching condition that the selectivity to the fourth and first insulating films 5 and 1 and the third insulating film 4 is high. Then, the contact hole CH is formed.

After the resist 6 is removed, the fifth insulating film 7 is deposited on the whole surface. When the whole surface of the fifth insulating film 7 is etch-backed by the RIE method, as shown in FIG. 2C, the side wall spacer 7a composed of the fifth insulating film 7 is formed on the side wall of the contact hole.

Also in this embodiment, the conductive film 2 is protected by the third insulating film 4. For this reason, at the time of etching by the RIE method, even if the alignment is not obtained on a mask, the conductive film 2 is not exposed. Therefore, even when a conductive layer is formed in the contact hole CH, the short-circuit between the conductive film 2 and the conductive layer can be prevented. Moreover, since

a thickness of the insulating film on the conductive film 2 is defined by the thicknesses of the second and third insulating films, controllability is satisfactory.

In the first and second embodiments, the material of the fifth insulating film 7 is, for example, silicon nitride film silicon oxide film, or a composite film of a silicon nitride film and a silicon oxide film. A dielectric constant of the fifth insulating film 7 is set smaller than a silicon nitride film.

FIGS. 3 and 4A through 4C show third embodiment of the present invention, and the parts described in the first and second embodiments are indicated by the same reference numerals. In FIGS. 4A through 4C, the semiconductor substrate is omitted. As shown in FIGS. 1A and 2A, the manufacturing steps up to the formation of the wiring L are the same as the first and second embodiments. The wiring L is formed by using a strip-like wiring pattern 8 shown in FIG. 3. Thereafter, the fourth insulating film 5 made of silicon oxide is deposited on the whole surface, and as shown in FIG. 4A, the fourth insulating film 5 is planarized with the upper surface of the third insulating film 4 by the CMP method.

Next, the photo-resist 6 shown in FIG. 4B is formed by using a linear/space contact hole pattern 9 which intersects perpendicularly to the wiring pattern 8 as shown in FIG. 3. Then, the fourth and first

insulating films 5 and 1 are etched by the RIE method under the etching condition that the selectivity to the fourth and first insulating films 5 and 1 and the third insulating film 4 is high, and a contact hole is formed between the wirings.

Next, the resist 6 is removed, and the fifth insulating film 7 is deposited on the whole surface. Then, the fifth insulating film 7 is etch-backed by the RIE method so that, as shown in FIG. 4C, the side wall space 7a is formed in the contact hole CH by the fifth insulating film 7. The widths of wiring pattern 8 and the contact hole pattern 9 are set to a minimum dimension which is defined by the design rule.

In this embodiment, since the conductive film 2 is protected by the third insulating film 4, at the time of etching by the RIE method, even if the alignment is not obtained on the mask, the conductive film 2 is not exposed. Therefore, even when a conductive layer is formed in the contact hole CH, the short-circuit between the conductive film 2 and the conductive layer can be prevented. Moreover, since the thickness of the insulating film on the conductive film 2 is defined by the thickness of the second and third insulating film, controllability is satisfactory. Moreover, since the contact hole pattern 9 has a linear/space shape, the contact hole can be easily formed. Further, when the linear/space contact hole pattern is used, the contact

hole has a square shape whose side has a minimum dimension defined by the design rule. Therefore, since the contact hole does not have a circular shape which is inscribed in a square shape having a minimum dimension side unlike the conventional manner, the contact area can be made larger, thereby decreasing the contact resistance.

The following describes fourth embodiment of the present invention on reference to FIG. 5, FIGS. 6A through 6J, FIGS. 7A through 7G, FIGS. 8A and 8B, and FIGS. 9A through 9E. The fourth embodiment relates to a case where the present invention is applied to a method of manufacturing the STC-type DRAM cell.

FIG. 5 is a plan view which shows a mask pattern applied to the fourth embodiment, and FIGS. 6A through 6J, FIGS. 7A through 7G, FIGS. 8A and 8B, FIGS. 9A through 9E show the steps of manufacturing the fourth embodiment. Namely:

FIGS. 6A and 7A show the first step;
FIGS. 6B and 7B show the second step;
FIGS. 6C and 7C show the third step;
FIGS. 6D and 7D show the fourth step;
FIGS. 6E and 7E show the fifth step;
FIGS. 8A and 7F show the sixth step;
FIGS. 8B and 7G show the seventh step;
FIGS. 6F and 9A show the eighth step;
FIGS. 6G and 9B show the ninth step;

FIGS. 6H and 9C show the tenth step;

FIGS. 6I and 9D show the eleventh step; and

FIGS. 6J and 9E show the twelfth step.

In FIG. 5, 101 represents an element separating pattern for forming an element separating region, 102 represents a gate electrode patter for forming a gate electrode, 103 represents a plug pattern for forming a plug, 104 represents a bit line contact pattern for forming a bit line contact, 105 represents a bit line pattern for forming a bit line, 106 represents a storage node contact pattern for forming a storage node contact, and 107 represents a storage node electrode pattern for forming a storage node electrode.

As shown in FIGS. 6A and 7C, an element separating oxide film 12 is formed on the semiconductor substrate 11 by using the STI (Shallow Trench Isolation) technique and using the element separating pattern 101 show in FIG. 5 as a mask.

Next, a gate oxide film, not shown, is formed on the semiconductor substrate 11. As shown in FIGS 6B and 7B, an N-type polysilicon film 13, a tungsten cilicide film 14 and a silicon nitride film 15 are deposited on the gate oxide film in this order. Thereafter, the silicon nitride film 15 and the tungsten silicide film 14 and the N-type polysilicon film 13 are patterned by using the gate electrode pattern 102 shown in FIG. 5, and an MOSFET gate

electrode G is formed. Next, ions as N-type impurity such as As are implanted into the semiconductor substrate 11 on the gate oxide film so that a source/drain diffusion layer 16 is formed. Thereafter, a silicon nitride film 17 is deposited on the whole surface, and the silicon nitride film 17 is etch-backed so that a side wall spacer 17a composed of the silicon nitride film is formed on the side wall of the gate electrode G.

Next, as shown in FIGS. 6C and 7C, a BPSG film 18 is deposited on the whole surface, and the surface of the BPSG film 18 is planarized by using the CMP method and using the silicon nitride film 15 as the stopper. Then, as shown in FIGS. 6D and 7D, a resist 19 is applied to the whole surface, and an etching mask 19a is formed by using the plug pattern 103 shown in FIG. 5 and using the lithography method. The BPSG film 18 is etched by using the RIE method and using the etching mask 19a and the silicon nitride film 15 as the mask under the etching condition that the selectivity to the BPSG film 18 and the silicon nitride film 15 is high. With this step, the contact hole 20 is formed so as to be self-aligned with the gate electrode G.

Next, after the resist 19 is removed, as shown in FIGS. 6E and 7E, an N-type polysilicon film 21 is deposited on the whole surface. Thereafter, the surface of the N-type polysilicon film 21 is planarized

by using the CMP method and using the silicon nitride film 15 and the BPSG film 18 as a stopper. At the same time, a plug 21a is formed in the contact hole 20 by the N-type polysilicon film 21.

As shown in FIG. 8A and 7F, a BPSG film 22 is deposited on the whole surface, and a contact hole 23 is formed by using the bit line contact pattern 104 shown in FIG. 5. The position of the contact hole 23 corresponds to the aforementioned contact hole 20. Next, a tungsten film 24 is selectively grown on the exposed N-type polysilicon thin film 21 so that the contact hole 23 is plugged up with the tungsten film 24.

A glue layer, not shown, is formed on the whole surface, and as shown in FIGS. 8B and 7G, a tungsten film 25, a silicon oxide film 26 and a silicon nitride film 27 are deposited in this order. Therefore, the silicon nitride film 27, the silicon oxide film 26, the tungsten film 25 and the glue layer are patterned by using the bit line pattern 105 shown in FIG. 5 so that a bit line BL connected to the plug 21 is formed.

Next, as shown in FIG. 6F and 9A, a silicon oxide film 28 is deposited on the whole surface, and the surface of the silicon oxide film 28 is planarized by using the CMP method and using the silicon nitride film 27 as a stopper. Then, a resist 29 is applied to the whole surface, and as shown in FIG. 6G, an etching mask

29a is formed by using the lithography method and using the storage node contact pattern 106 shown in FIG. 5. Thereafter, the silicon oxide film 28 is etched by using the RIE method and using the etching mask 29a and the silicon nitride film 27 as a mask. The etching condition in this case is such that the selectivity of the silicon oxide film 28 and the silicon nitride film 27 is high. With this step, a contact hole 30 is formed so as to be self-aligned with the bit line BL.

After the resist 29 is removed, as shown in FIGS. 6H and 9C, a silicon oxide film 31 is deposited on the whole surface. Thereafter, a side wall spacer 31a composed of the silicon oxide film 31 is formed on the side wall of the contact hole 30 by using the etch-back method. As shown in FIGS. 6I and 9D, an N-type polysilicon film 32 is deposited on the whole surface, and the surface of the N-type polysilicon film 32 is planarized by using the CMP method and using the silicon nitride film 27 and the silicon oxide film 28 as a stopper. At the same time, a plug 32a is formed in the contact hole 30 by the N-type polysilicon film 32.

Next, as shown in FIGS. 6J and 9E, a ruthenium film 33 is deposited on the whole surface by the sputtering method, and it is patterned by using the storage node electrode pattern 107 shown in FIG. 5. Thereafter, a high dielectric film such as a BST

(Barium Strontium Titanate) film 34 and a ruthenium film 35 are deposited on the whole surface, and a storage capacitor is formed. Then, a wiring layer, etc., not shown, is formed by a know method, and thus the DRAM is finished.

In accordance with the fourth embodiment, in the STC-type DRAM cell, the bit line is protected by a silicon nitride insulating film. For this reason, even if the storage node contact pattern is not aligned with the bit line pattern, exposure of the bit line can be prevented at the time of etching. Moreover, since the insulating film on the bit line is defined by its thickness, the controllability is satisfactory.

In addition, since the storage node contact pattern has a line/space shape, the storage node contact can be prevented from becoming round, thereby making it possible to make the shape of the storage node contact a square whose side has a minimum dimension. Therefore, the contact area can be made large, thereby decreasing the contact resistance.

In addition, since the storage node contact does not reach the substrate and it is connected to the source/drain domain through the conductive plug, an aspect ratio can be lowered. Therefore, the storage node can be easily plugged up, and thus the yielding of the contact opening can be improved.

Furthermore, when the silicon oxide insulating

film is used as the side wall spacer, the capacity of the bit line can be prevented from increasing, thereby increasing a higher operating speed and decreasing current consumption.

FIGS. 10A and 10B show fifth embodiment of the present invention. Here, the parts shown in FIGS. 1A through 4C are indicated by the same reference numerals, and only parts not shown in FIGS. 1A through 4C are described. In the second and third embodiments, the second insulating film 3 and the third insulating film 4 (in the fourth embodiment, the silicon oxide film 26 and the silicon nitride film 27) are provided on the conductive layer 2. The material of the third insulating film 4 (in the fourth embodiment, the silicon nitride film 27) has the following conditions:

(1) when the silicon oxide film is subject to RIE, the selectivity with the silicon oxide film is large;

(2) when the silicon oxide film is subject to CMP, the selectivity with the silicon oxide film is large;

(3) when the plug is subject to CMP, the selectivity with the plug is large; and

(4) an insulating film.

However, as mentioned above, the third insulating film 4 (in the fourth embodiment, the film 27) is composed of the silicon nitride film. The silicon nitride film has a large capacity and decreases the speed of signal transfer through the wiring.

Therefore, it is desirable to remove the silicon nitride film.

Therefore, in the fifth embodiment, when the fifth insulating film 7 is etch-backed, the etching time is made slightly longer, and as shown in FIG. 10A, the fifth insulating film 7 formed on the side wall of the third insulating film 4 is removed. Thereafter, as shown in FIG. 10B, the third insulating film 4 is removed by the process using thermal phosphoric acid. The same effects as the first through fourth embodiments can be obtained in the present embodiment, and decrease the speed of signals transfer through the wiring can be obtained. In such a manner, when the third insulating film is removed, the above-mentioned conditions (3) and (4) are not necessary. The present embodiment explains the case of the silicon nitride film, but a conductive film such as polysilicon may be used.

FIGS. 11A through 11C show sixth embodiment of the present invention. In the first through fifth embodiments, the third insulating film 4 is provided on the second insulating film 3, but a conductive film can be provided on the second insulating film 3 as long as the conditions (1) and (2) are satisfied. In the sixth embodiment, a polysilicon film 41 is provided on the second insulating film 3. Since the polysilicon film 41 has a higher selectivity with the silicon oxide

film, like the first through fourth embodiments, when the silicon oxide film 5 is etched, the wiring can be protected. However, since the polysilicon film 41 has conductivity, it should be removed in order to avoid a short-circuit with another film.

Therefore, as shown in FIG. 11A, the fifth insulating film 7 formed on the side wall of the polysilicon film 41 is removed like the fifth embodiment. Next, as shown in FIG. 11B, a polysilicon film 42 is deposited on the whole surface. Thereafter, as shown in FIG. 11C, the polysilicon films 41 and 42 are removed by the CMP method, and the contact hole is plugged up by the polysilicon film 42. At this time, the silicon oxide film 3 functions as a stopper. The same effects as the fifth embodiment can be obtained in the present embodiment.

FIG. 12 shows seventh embodiment of the present invention, more specifically, a modification of the sixth embodiment. In the present embodiment, a ruthenium film 43, for example, is formed on the second insulating film 3, and a ruthenium film 44 is deposited on the whole surface. Next, in order to manufacture an electrode, the ruthenium film 44 is etched by using a predetermined pattern, and the ruthenium film 44 as well as the ruthenium film 43 is removed.

The film on the second insulating film 3 and the film deposited on the whole surface are made of

ruthenium. For this reason, when manufacturing an electrode, even if the pattern is slightly misaligned as shown in FIG. 12, no problem arises.

In addition, the material of the film on the second insulating film 3 is not limited to ruthenium, so a metallic film, for example, which is similar to the film 44 deposited on the whole surface may be used as long as the aforementioned conditions (1) and (2) are satisfied.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

What is claimed is:

1. A semiconductor storage device comprising:

a first insulating film formed on a semiconductor substrate;

first and second wirings arranged on said first insulating film at a predetermined interval, said first and second wirings composed of a conductive film, and a second insulating film on the conductive film;

a contact hole formed between said first and second wirings, and in said first insulating film between said first and second wirings; and

a third insulating film formed in said contact hole, said third insulating film being formed at least on a side wall of the conductive film and a side wall of said first insulating film.

2. A device according to claim 1, wherein said second insulating film is a silicon nitride film, and said first insulating film is a silicon oxide film.

3. A device according to claim 1, wherein said third insulating film is a silicon nitride film.

4. A device according to claim 1, wherein said third insulating film is a silicon oxide film or a composite film of a silicon nitride film and a silicon oxide film, and has a smaller dielectric constant than a silicon nitride film.

5. A semiconductor storage device comprising:

an MOS transistor having a gate electrode and

a source/drain region, said MOS transistor being formed on a surface of a semiconductor substrate;

a bit line connected to one region of said source/drain region, said bit line being located so as to intersect perpendicularly to a word line connected to said gate electrode;

a capacitor formed above said bit line, said capacitor being connected to the other region of said source/drain region;

a first insulating film covering said MOS transistor, said bit line being located on said first insulating film;

a second insulating film formed on said bit line;

a third insulating film formed on said first insulating film and said second insulating film;

a contact hole for forming a storage node electrode of said capacitor formed through said third insulating film and said first insulating film, said contact hole exposing a side face of said bit line; and

a fourth insulating film formed at least on a side wall of said bit line exposed from said contact hole and a side wall of said first insulating film.

6. A device according to claim 5, wherein said third insulating film is a silicon nitride film, and said second and fourth insulating films are silicon oxide film.

7. A device according to claim 5, wherein said

fourth insulating film is a silicon oxide film or a composite film of a silicon nitride film and a silicon oxide film, and has a smaller dielectric constant than a silicon nitride film.

8. A device according to claim 5, wherein said contact hole for said storage node is divided by a linear/space pattern which intersects perpendicular to said bit line.

9. A semiconductor device comprising:

an MOS transistor having a gate electrode and a source/drain region, said MOS transistor being formed on a surface of a semiconductor substrate;

a bit line connected to one region of said source/drain region, said bit line being located so as to intersect perpendicularly to a word line connected to said gate electrode;

a capacitor formed above said bit line, said capacitor being connected to the other region of said source/drain region;

a first insulating film covering said MOS transistor, said bit line being located on said first insulating film;

a second insulating film formed on said bit line;

a conductive film formed on said second insulating film;

a third insulating film formed on said first insulating film and said conductive film;

a contact hole for forming a storage node electrode of said capacitor formed through said third insulating film and said first insulating film, said contact hole exposing a side face of said bit line;

a fourth insulating film formed at least on a side wall of said bit line exposed from said contact hole and a side wall of said first insulating film; and

a storage node electrode connected to one part of said conductive film, said storage node electrode being electrically separated by said bit line and said fourth insulating film.

10. A device according to claim 9, wherein said fourth insulating film is a silicon oxide film or a composite film of a silicon nitride film and a silicon oxide film, and has a smaller dielectric constant than a silicon nitride film.

11. A device according to claim 9, wherein said contact hole for the storage node is divided by a linear/space pattern which is intersects perpendicularly to said bit line.

12. A semiconductor storage device comprising:

a semiconductor substrate;

an element separation insulating film, formed on said semiconductor substrate, for dividing an element region;

an MOS transistor, formed in the element region, having a gate insulating film, a gate electrode

connected to a word line and a source/drain region;

a first insulating film covering said element separation insulating film and said MOS transistor;

a first contact hole, formed on said first insulating film, reaching one source/drain region of said MOS transistor;

a second contact hole, formed on said first insulating film, reaching the other source/drain region of said MOS transistor;

a first conductive plug for filling up said first contact hole;

a second conductive plug for filling up said second contact hole;

a second insulating film covering said first insulating film and said first and second conductive plugs;

a bit line contact, formed on said second insulating film, reaching said first conductive plug;

a bit line formed on said second insulating film and bit line contact, a lower part of said bit line being composed of a conductive film and an upper part being composed of a third insulating film;

a fourth insulating film formed on said second insulating film and bit line;

a contact hole for storage node, located on the side of said bit line and formed through said fourth insulating film and said second insulating film, said

contact hole reaching said second conductive plug;

a fifth insulating film formed at least on a side wall of said conductive film and a side wall of said second insulating film on said bit line exposed from said contact hole; and

a capacitor connected to said second conductive plug, said capacitor having a storage node electrode electrically separated by said conductive film on said bit line connected to said second conductive plug and said fifth insulating film, and a capacitor insulating film on the storage node electrode and a plate electrode on the capacitor insulating film.

13. A device according to claim 12, wherein said third insulating film is a silicon nitride film, and said second and fourth insulating films are silicon oxide films.

14. A device according to claim 12, wherein said fifth insulating film is a silicon oxide film or a composite film of a silicon nitride film and a silicon oxide film, and has a smaller dielectric constant than a silicon nitride film.

15. A device according to claim 12, wherein said contact hole for a storage node is divided by a linear/space pattern which intersects perpendicularly to said bit line.

16. A semiconductor storage device comprising:

a semiconductor substrate;

element separation insulating films, formed on said semiconductor substrate, for dividing element region;

a plurality of MOS transistors formed in the element regions, said MOS transistors respectively have a gate insulating film, a gate electrode connected to a word line and a source/drain region;

a first insulating film for covering said element separation insulating films and said MOS transistors;

first contact holes, formed on said first insulating film, reaching one source/drain regions of said MOS transistors;

second contact holes, formed on said first insulating film, reaching the other source/drain regions of said MOS transistors;

a first conductive plug for filling up said respective first contact holes;

a second conductive plug for filling up said respective second contact holes;

a second insulating film for covering said first insulating film and said first and second conductive plugs;

a bit line contact, formed on said second insulating film, reaching said respective first conductive plugs;

bit lines formed respective on said second insulating film and said bit line contact, an lower

part of said respective bit lines being composed of a conductive film and upper part being composed of said third insulating film;

a fourth insulating film formed on said second insulating film and said bit lines;

a contact hole for a storage node, locating between said bit lines and formed through said fourth insulating film and said second insulating film, said contact hole reaching said second conductive plug;

a fifth insulating film formed at least on a side wall of said conductive film and a side wall of said second insulating film on said bit line exposed from said contact hole;

a capacitor connected to said second conductive plug, said capacitor having a storage node electrode electrically separated by the conductive film and said fifth insulating film on said bit line connected to said second conductive plug, a capacitor insulating film on the storage node electrode and a plate electrode on the capacitor insulating film.

17. A device according to claim 16, wherein said third insulating film is a silicon nitride film, and said second and fourth insulating films are silicon oxide films.

18. A device according to claim 16, wherein said fifth insulating film is a silicon oxide film or a composite film of a silicon nitride film and a silicon

oxide film, and has a smaller dielectric constant the a silicon nitride film.

19. A device according to claim 16, wherein said contact hole for the storage node is divided by a linear/space pattern which intersects perpendicularly to said bit lines.

20. A method of manufacturing a semiconductor storage device comprising the steps of:

forming a first insulating film on a semiconductor substrate;

forming a conductive film on said first insulating film;

forming a protective film on said conductive film;

etching said protective film and conductive film locally and forming first and second wirings;

forming a second insulating film between said first and second wirings;

etching said second insulating film and first insulating film locally by using said protective film as a mask and forming a contact hole between said first and second wirings; and

forming a third insulating film at least on a side wall of said conductive film and on a side wall of said first insulating film in said contact hole.

21. A method according to claim 20, said step of forming said second insulating film between said first and second wirings comprises the steps of:

depositing said second insulating film on a whole surface; and

etching said second insulating film up to the upper surface of said protective film and removing it and planarizing the surface.

22. A method according to claim 20, wherein said step of etching said second and first insulating films locally using said protective film as a mask and forming said contact hole between said first and second wirings comprises the steps of:

forming a linear/space photo-resist which intersects perpendicularly to said first and second wirings; and

etching said second and first insulating films locally using said photo-resist and protective film as a mask.

23. A method according to claim 20, wherein said protective film is composed of a silicon nitride film, and the silicon nitride film is removed after said third insulating film is formed.

24. A method according to claim 20, wherein said protective film is composed of one of a second conductive film and a metallic film, and one of the second conductive film and the metallic film is removed after said third insulating film is formed.

25. A method according to claim 20,

wherein said protective film is composed of

a second conductive film,

wherein said step of forming said protective film comprises the step of forming a third conductive film on said second conductive film, said second insulating film and in said contact hole after said third insulating film is formed, and the step of etch-backing said third and second conductive films and removing said second conductive film and filling up said contact hole with said third conductive film.

26. A method according to claim 20,

wherein said protective film is composed of a second conductive film,

said step of forming said protective film comprises the step of forming a third conductive film on said second conductive film and said second insulating film and in said contact hole after said third insulating film is formed, and the step of etching and removing a portion of said third and second conductive films when said third conductive film is patterned by using a predetermined storage node electrode pattern.

27. A method of manufacturing a semiconductor storage device comprising steps of:

forming an element separation insulating film on a semiconductor substrate, for dividing an element region;

forming a gate electrode on the element region

divided by said element separation insulating film, connected to a gate insulating film and a word line, and an MOS transistor having a source/drain region;

forming a first insulating film for covering said MOS transistor and said element separation insulating film;

etching said first insulating film locally and forming a first contact hole reaching one of the source/drain regions of said MOS transistor and a second contact hole reaching the other source/drain region of said MOS transistor, said first contact hole being formed on the element region and on said element separation insulating film, and said second contact hole being formed on the element region, said first and second contact holes being self-aligned with said gate electrode;

forming first and second conductive plug for filling up said first and second contact holes;

forming a second insulating film for covering said first insulating film and said first and second conductive plug;

etching said second insulating film locally and forming a bit line contact reaching said first conductive plug on said element separation insulating film;

forming a bit line, whose lower section is composed of a conductive film and upper section is

composed of a third insulating film, on said second insulating film and said bit line contact;

forming a fourth insulating film on said second insulating film and said bit line;

etching said fourth insulating film and said second insulating film locally by using said third insulating film as a mask and forming a storage node contact reaching said second conductive plug so that said storage node contact is self-aligned with said bit line;

forming a fifth insulating film on a side wall of the conductive film of said bit line and a side wall of said second insulating film in said storage node contact; and

forming a storage node electrode, a capacitor insulating film on said storage node electrode and a plate electrode on said capacitor insulating film in this order so as to form a capacitor, said storage node electrode connected to said second conductive plug and electrically separated from the conductive film of said bit line by said fifth insulating film.

28. A method according to claim 27, wherein said step of forming said fourth insulating film on said second insulating film and said bit line comprises the step of:

depositing said fourth insulating film on the whole surface; and

etching and removing said fourth insulating film up to an upper surface of said third insulating film so as to level the surface.

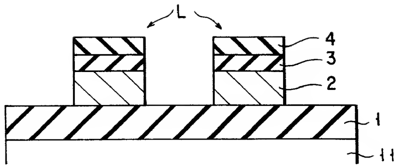
29. A method according to claim 27, wherein said step of etching said fourth insulating film and said second insulating film locally by using said third insulating film as a mask and forming a storage node contact reaching said second conductive plug so that said storage node contact is self-aligned with said bit line, comprises the steps of:

forming a linear/space photo-resist which intersects perpendicularly to said bit line; and

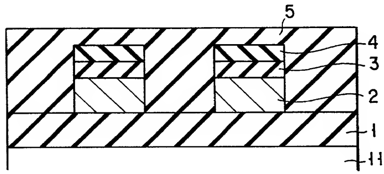
etching said fourth insulating film and said second insulating film locally by using said photo-resist and said third insulating film as a mask.

Abstract of the Disclosure

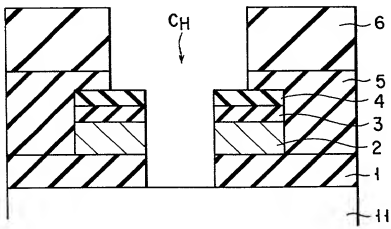
First and second wirings are formed on a first insulating film. Each of the wirings is arranged so that a conductive film, a silicon oxide film and a silicon nitride film are laminated. Thereafter, a silicon oxide insulating film on the whole surface. The silicon oxide insulating film is etched so that a contact hole is formed between the first and second wirings. Since the silicon oxide film and the silicon nitride film exist on the conductive film of each wiring, the conductive film is not exposed at the time of etching. Thereafter, an insulating film is formed on a side wall of the contact hole, and the conductive film exposed through the contact hole is covered by the insulating film.



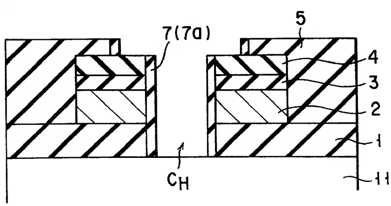
F I G. 1A



F I G. 1B



F I G. 1C



F I G. 1D

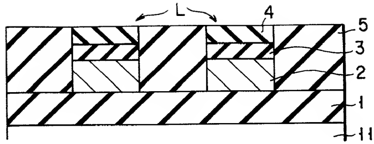


FIG. 2A

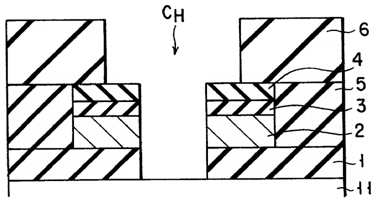


FIG. 2B

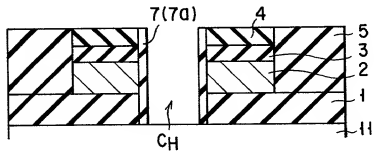


FIG. 2C

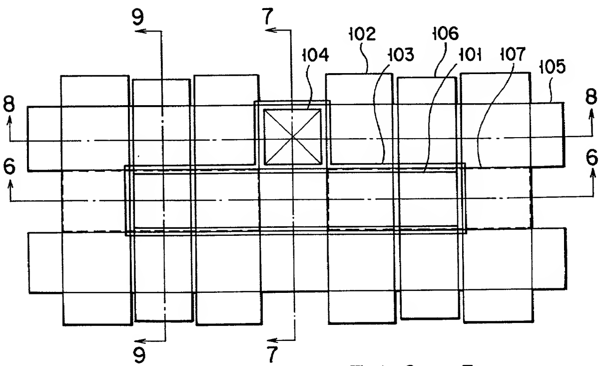


FIG. 5

FIG. 3

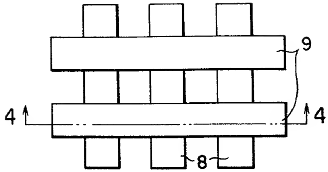


FIG. 4A

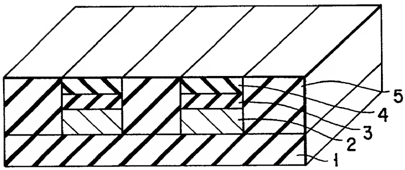


FIG. 4B

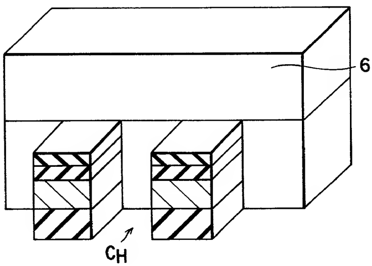
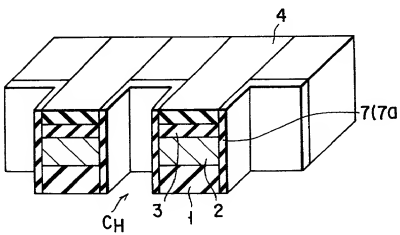
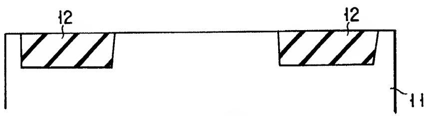
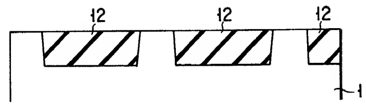


FIG. 4C

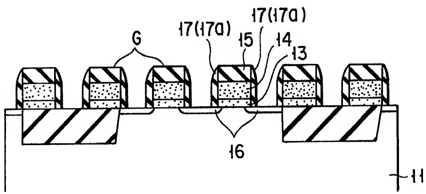




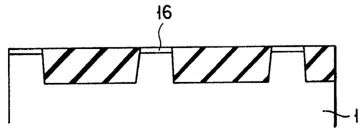
F I G. 6A



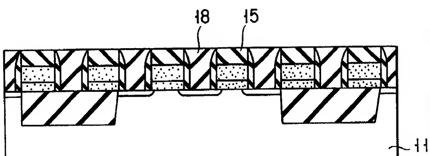
F I G. 7A



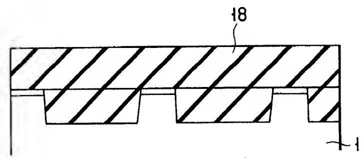
F I G. 6B



F I G. 7B



F I G. 6C



F I G. 7C

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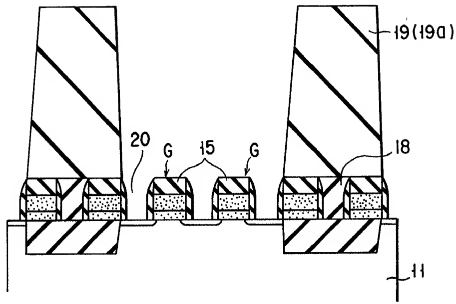


FIG. 6D

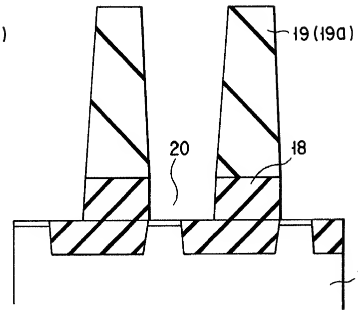


FIG. 7D

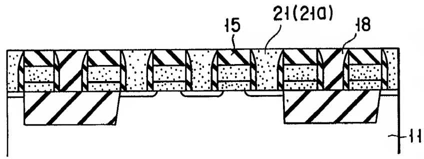


FIG. 6E

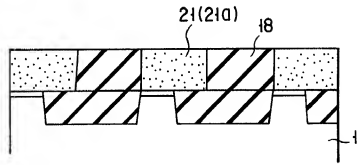


FIG. 7E

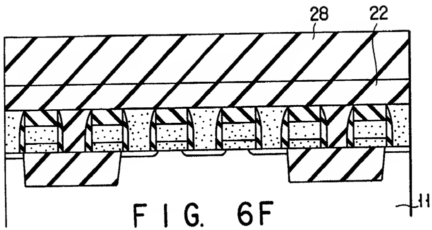


FIG. 6F

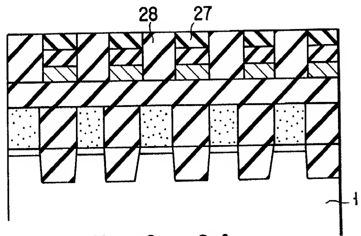


FIG. 9A

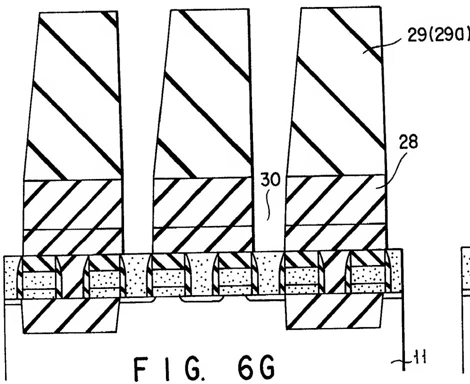


FIG. 6G

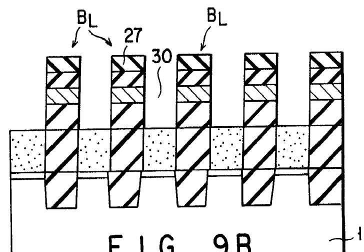
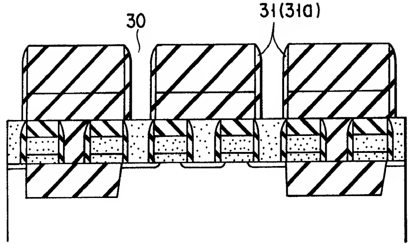
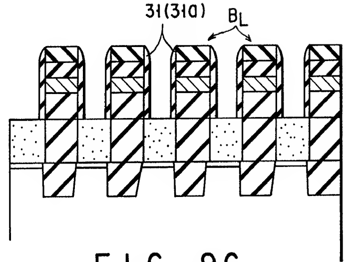


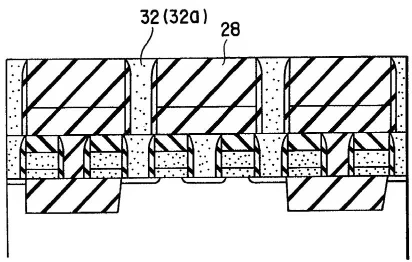
FIG. 9B



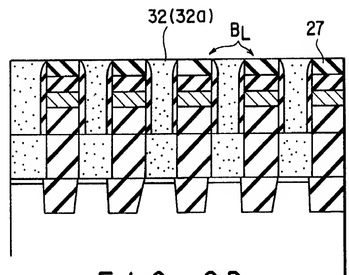
F I G. 6H



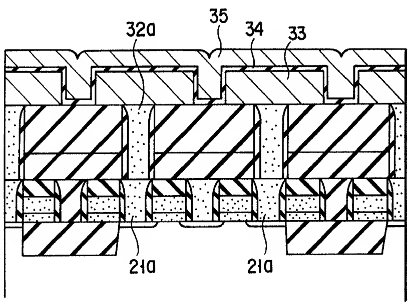
F I G. 9C



F I G. 6I



F I G. 9D



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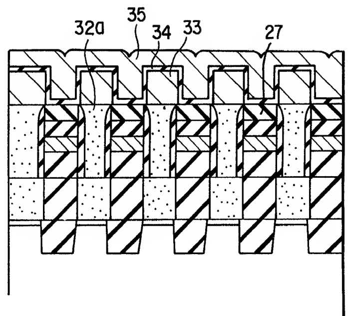
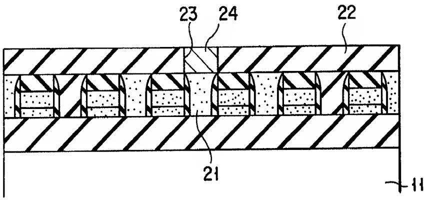
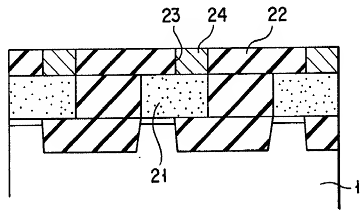


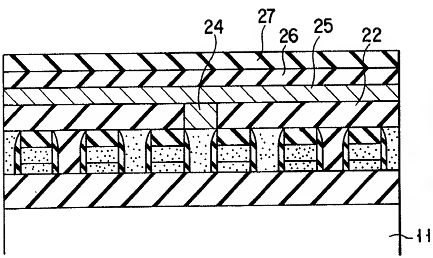
F I G. 9E



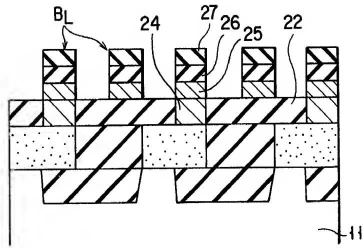
F I G. 8A



F I G. 7F



F I G. 8B



F I G. 7G

FIG. 10A

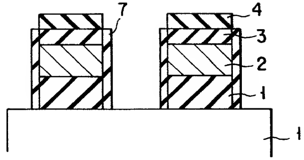


FIG. 10B

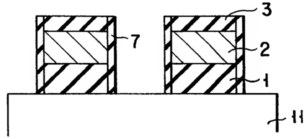


FIG. 11A

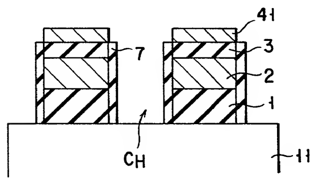


FIG. 11B

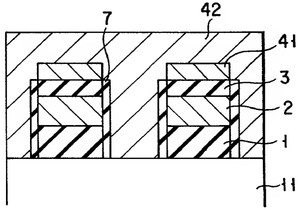
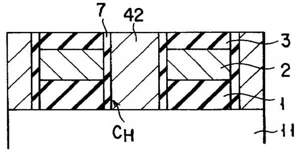
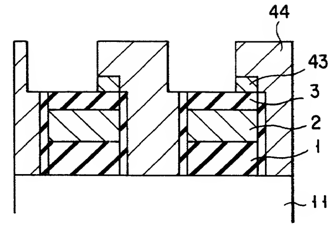
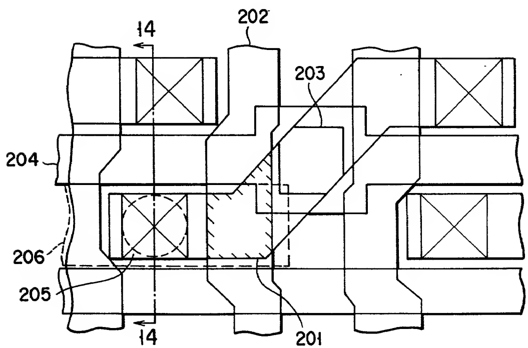


FIG. 11C





F I G. 12



F I G. 13
(PRIOR ART)

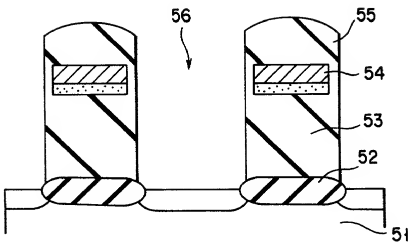


FIG. 14A
(PRIOR ART)

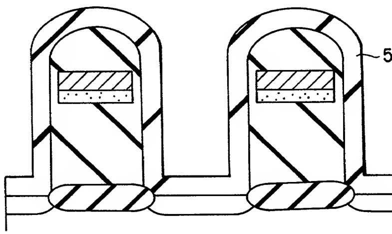


FIG. 14B
(PRIOR ART)

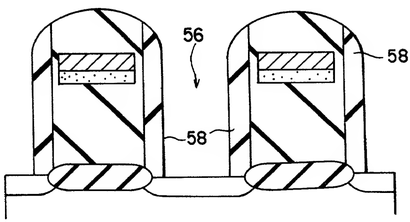


FIG. 14C
(PRIOR ART)

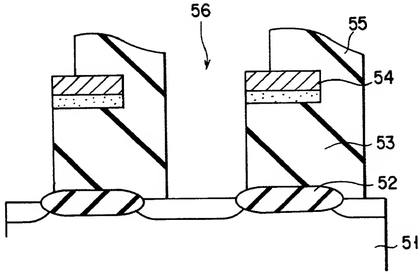


FIG. 15A
(PRIOR ART)

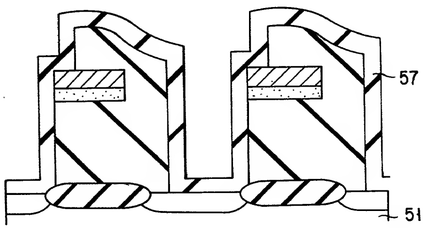


FIG. 15B
(PRIOR ART)

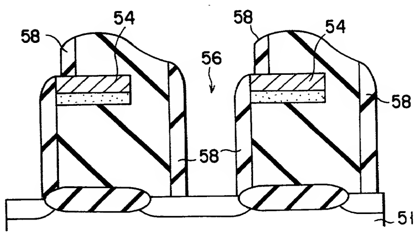


FIG. 15C
(PRIOR ART)

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I declare:
that I verily believe myself to be the original, first and sole (if only one individual inventor is listed below) or an original, first and joint inventor (if more than one individual inventor is listed below) of the invention in

STACKED CAPACITOR-TYPE SEMICONDUCTOR STORAGE DEVICE AND MANUFACTURING METHOD THEREOF

the specification of which is attached hereto unless the following box is checked.

☐ was filed on ____________ as United States Application or PCT International Application No.____________, and was amended on ____________ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.
I acknowledge the duty to disclose information of which is material to patentability as defined in 37 CFR 1.56.
I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365 (b) of any foreign application(s) for patent or inventor's certificate, or 35 U.S.C. 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Country	Category	Application No.	Filing Date	Priority Claim
Japan	Patent	7-254218	September 29, 1995	Yes

And I hereby appoint Donald W. Banner (Reg. No. 17,037), Harold J. Birch (Reg. No. 16,527), Edward F. McKie, Jr. (Reg. No. 17,335), William W. Beckett (Reg. No. 18,262), Dale H. Hoscheit (Reg. No. 19,090), Joseph M. Potenza (Reg. No. 28,175), Alan I. Cantor (Reg. No. 28,163), James A. Niegowski (Reg. No. 28,331), Barry L. Grossman (Reg. NO. 30,844), Joseph M. Skerpon (Reg. No. 29,864), Thomas L. Peterson (Reg. No. 30,969), Nina L. Medlock (Reg. No. 29,673), William J. Fisher (Reg. No. 32,133) and Thomas H. Jackson (Reg. No. 29,808), each of whose address is 11th Floor, 1001 G Street, N.W., Washington, D.C. 20001-4597, or any one of them, my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent & Trademark Office connected therewith, and request that correspondence be directed to Banner & Allegretti, Ltd., 11th Floor, 1001 G Street, N.W., Washington, D.C. 20001-4597.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

96S0200

DECLARATION FOR PATENT APPLICATION

I declare further that my post office address is at c/o Intellectual Property Division, KABUSHIKI KAISHA TOSHIBA, 1-1 Shibaura 1-chome, Minato-ku, Tokyo 105, Japan; and that my citizenship and residence are as stated below next to my name:

Inventor: (Signature)	Date	Residence
Yusuke Kohyama Yusuke Kohyama	Date: SEP 18.1996 Citizen of: Japan	Yokosuka-shi, Kanagawa-ken, Japan
Takashi Ohsawa Takashi Ohsawa	Date: SEP 18.1996 Citizen of: Japan	Yokohama-shi, Japan
Shizuo Sawada Shizuo Sawada	Date: SEP. 18.1996 Citizen of: Japan	Urawa-shi, Saitama-ken, Japan
	Date: Citizen of: Japan	
	Date: Citizen of: Japan	
	Date: Citizen of: Japan	
	Date: Citizen of: Japan	
	Date: Citizen of: Japan	